SAVING CACHE MEMORY USING A LOCKING CACHE IN REAL-TIME SYSTEMS

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ABSTRACT – Locking cache is a practical alternative to traditional caches in real-time systems. With similar performance than conventional caches, a locking cache allows a simple, accurate schedulability analysis. This work presents a new application of the locking cache. Along the modern trend to design Systems-On-a-Chip (SOCs) in which a single IC, usually a programmable device like an FPGA, is designed with one or more microprocessors and peripherals, a locking cache is used to reduce the cache size to the minimum that satisfies the system schedulability. Although results are not as good as the authors expected, the developed technique is promising, and future work may lead to very interesting cost reductions in the size of the memory hierarchy of real-time systems while maintaining their schedulability properties.

KEYWORDS: Cache memories, Locking cache, Cost aware, Real-Time systems, System on a Chip etc

References


